Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-17 (Canceled)

Claim 18 (Currently Amended): A non-volatile memory array having vertical transistors, wherein each of the vertical transistors is formed in a trench of a semiconductor substrate and comprises:

a first doping region of a first conductive type being underneath a bottom of the trench;

a second doping region of the first conductive type being beside a top of the trench;

a third doping region of a second conductive type beside the trench;

a fourth doping region of the first conductive type beside the trench, and being located lower than the third doping region;

a gate dielectric layer formed on a surface of the first doping region, an upper surface of the second doping region and a sidewall of the trench, wherein the gate

dielectric layer comprises at least one nitride film; and

a conducting plug formed in the trench,

wherein the first doping regions of the vertical transistors are connected as a common plate serving as one of a common source and a common drain.

Claim 19 (Original): The non-volatile memory array having vertical transistors of Claim 18, wherein the semiconductor substrate is constituted of a silicon substrate and a mask layer.

Claim 20 (Original): The non-volatile memory array having vertical transistors of Claim 19, wherein the mask layer is selected from the group of silicon nitride, silicon oxide, silicon oxynitride and multi-layer thereof.

Claim 21 (Original): The non-volatile memory array having vertical transistors of Claim 19, wherein the mask layer is of a thickness between 100 to 2000 angstroms.

Claim 22 (Previously Presented): The non-volatile memory array having vertical transistors of Claim 18, wherein the first and second doping regions function as bit lines

for the non-volatile memory array.

Claim 23 (Original): The non-volatile memory array having vertical transistors of Claim 18, wherein the gate dielectric layer is an oxide/nitride/oxide layer.

Claim 24 (Original): The non-volatile memory array having vertical transistors of Claim 23, wherein the oxide/nitride/oxide layer is of a thickness between 60-500 angstroms.

Claim 25 (Previously Presented): The non-volatile memory array having vertical transistors of Claim 18, wherein the conducting plug is a polysilicon plug.

Claim 26 (Currently Amended): The non-volatile memory array having vertical transistors of Claim 18, wherein each ~~the at least one~~ of the vertical transistors further comprises insulation blocks formed on surfaces of the first and second doping regions.

Claim 27 (Currently Amended): The non-volatile memory array having vertical

transistors of Claim 26, wherein each ~~the at least one~~ of the vertical transistors further comprises edge insulation layers formed on sidewalls of the trench, and the insulation blocks are thicker than the edge insulation layers.

Claims 28-32 (Canceled)